Electronics and Communication Engineering

Short Term Training Programs

KARNATAK LAW SOCIETY's

VISHWANATHRAO DESHPANDE RURAL INSTITUTE OF TECHNOLOGY

HALIYAL - 581 329

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Presents

SHORT TERM HANDS ON TRAINING PROGRAMS

FOR DIPLOMA STUDENTS IN SUBJECTS LIKE

ARDUINO Programming

VERILOG - HDL

PCB Design

We Cordially welcome all the student participants from other colleges

Prof. Raveendra Moodithaya
Head, Dept of ECE,
KLS VDRIT, Haliyal

Dr. V. V. Katti
Principal,
KLS VDRIT, Haliyal

Department of Electronics & Communication Engineering KLS VDRIT, Haliyal organized Short Term Training Programme on "VERILOG HDL with Hands on" from 01/01/2018 to 12/01/2018. The main objective of the STTP was to create awareness among all the students of polytechnic college regarding advancements in the field of Electronics and Communication by organizing hands on sessions. The program emphasized on Introduction to Verilog language and writing dataflow, gate-level and behavioral source codes. The workshop followed insightful lectures and practical approach to impart Hands-on experience with efficient use of Verilog HDL with industry standard cutting edge tools like Xilinx ISE and targeting the deigns on FPGA Boards.

The program will be of immense benefit to all those who are planning to pursue higher education, academic projects etc.
Resource persons for the Course:
1. Prof. Meenaxi Torase
2. Prof. Vikas Balikai
3. Prof.Jyothi B R
4. Prof. Nikhil Kulkarni
Lab Instructor: Mr. Manjunath M

COURSE CONTENTS:

MODULE 1 (2 Hours)	❖ Basic Logical gates, Boolean expressions, ❖ Half Adder and Full adder circuits ❖ Multiplexer, De-Mux, ❖ Encoder, Priority Encoder, Decoder ❖ Binary to Gray, Comparator circuit
MODULE 2 (Theory-6Hrs Lab -6Hrs)	❖ Language introduction ❖ Difference between VHDL and Verilog ❖ Levels of abstraction ❖ Module, Ports types and declarations ❖ Registers and nets, Arrays ❖ Identifiers, Parameters ❖ Relational, Arithmetic, Logical, Bit-wise shift Operators. ❖ Lexical conventions, data types ❖ System tasks, compiler directives. ❖ Writing expression. ❖ Behavioral Modeling ❖ Structural Coding

MODULE 3 (Theory-6Hrs, Lab -6Hrs)	❖ Assign statements ❖ Continuous Assignments ❖ Always, Initial Blocks, begin end, fork join. ❖ Gate Instantiation, ❖ Gate types: and/or, buf/not gates, bufif/notif gates ❖ Gate delays ❖ Procedural Statements-Blocking and Non-blocking statements ❖ Conditional Statements-If,else ❖ Multi-way Branching case, Casex ❖ Loops: while, for-loop, forever, repeat ❖ Sequential and Parallel Blocks. ❖ Includes appropriate lab sessions along with interfacing with spartan 3e kit

COLLEGE NAME	DURATION	NO. OF PARTICIPANTS
K. H. Kabbur Polytechnic, Dharwad	01/01/2018 - 04/01/2018	61
Shree Vidyadhiraj Polytechnic, Kumta	04/01/2018 - 06/01/2018	37
SUC Polytechnic, Dandeli	08/01/2018 - 10/01/2018	4
Govt. Polytechnic, Joida	08/01/2018 - 10/01/2018	15
Gangadhar Polytechnic, Dharwad	10/01/2018 - 12/01/2018	6
S.G.E.E.S Rural Polytechnic, Tarihal	10/01/2018 - 12/01/2018	34
Government Polytechnic For Women,Hubli	22/01/2018 - 24/01/2018	58

The course started with an Inauguration function which was attended by,

- **Dr.V.V.Katti** Principal KLS VDRIT, Haliyal as Chief Guest, in his inaugural speech addressed the students and insisted them to enhance their technical skills through this STTP.
- **Prof.Raveendra Moodithaya** H.O.D ECE Department as President, told the importance of verilog programming in semiconductor industry.
- **Prof. Vikas Balikai** Faculty ECE Department as Course Coordinator.
- **Prof. Meenaxi Torase** Faculty ECE Department as Course Coordinator.
- **Prof. Jyothi B R** Faculty ECE Department as Course Coordinator.
- **Prof. Nikhil Kulkarni** Faculty ECE Department as Course Coordinator

Participation certificates were issued to all the participants on successful completion of course.

Principal, Dr.V.V.Katti addressing
K.H. Kabbur, Dharwad

Principal, Dr.V.V.Katti addressing Shree
Vidyadhiraj polytechnic, Kumta

Head of ECE Dept, Prof. Raveendra M
Addressing the students

Hands On Session during STTP

Principal,Dr V.V.Katti addressing the Students
during valedictory

Certificates were issued to all participants

Hands-on Training for Government Polytechnic For Women,Hubli

Certificates were issued to all participants

Participants and staff of VDRIT

Department of Electronics and Communication Engg. has conducted a Student Technical Training Program (STTP) for students.

Students from 6th and 8th semester ECE of our college have participated in these Training Programs.

From the Dept of Electronics & Communication Engineering, faculty members conducted training programs on Network Simulator-2 and Open Secure Socket Layer which includes both theory and lab sessions.

The STTP Commenced with an Inaugural Function, Prof A S Joshi delivered Welcome Speech, Principal Dr. V. V. Katti, in his Inaugural speech addressed students and insisted them to utilize the facilities of the college and aquire better knowledge by these opportunities.

STTP was Organized On 25th February 2018, for 8th semester ECE Students on Open Secure Socket Layer and the resource Person was Dr. B R Chandavarkar from NITK Surthkal. He explained the students about Introduction to Cryptography and network security and OPENSSL Installation procedure, Introduction to OPENSSL with Symmetric Ciphers and Asymmetric Ciphers, HTTP and HTTPS using OpenSSL.

STTP was Organized On 26th February 2018, for 6th semester ECE Students on Network Simulator-2 and the resource Person was Dr. B R Chandavarkar from NITK Surthkal. He explained the students about Introduction to Computer Networks and Introduction to Network Simulator-2, Installation procedure, TCL and OTCL programming,NS-2 Programming.

The Student Technical Training Program (STTP) session was concluded by a valedictory function and certificates were issued to the students by Resource Person.

Events

Invited Talks

Dr. S.K Bhat

On 23rd March 2018 Department Of E&C arranged an expert talk on Satellite, its evolution and challenges. Dr S K Bhat of ISRO addressed the students of final year.

Prof Raveendra M HOD E&C Department was the president of the function.

Dr S K Bhat , senior scientist of ISRO in his address to the students explained the evolution of the microprocessor and how interrupts are avoided in the satellite. He also explained the importance of real time systems and feedback control system as well as about the self correcting feature of satellites.

Prof Rohini Kallur Hosted the function.

AAvishkaar 2018

Master Mind :

Round 1 is Quick Thinker, in which teams should solve the given puzzle within the time duration Top 20 teams will be selected for next round.

2) Round 2 is Remember!, in which each team should find objects in the shown image within time duration. Top 10 will be selected for next round.

3) Round 3 is WhoAmI?, in which teams will be asked to identify celebrities shown within time duration, Top 5 will be selected for next round.

4) Round 4 is DoYouKnowMe?, in which teams will be asked to guess the object based on the given description. Highest scoring 2 teams will be awarded.

Rules for individual round with Time duration will be given on site.

>Maximum team size - 2

>Venue - Edusat Seminar Hall

Esparta again:

Event Theme: It's a non Technical gaming event, where in the students will form a team of 3 members and they need to take first round which will be an elimination round. The team completing first will assemble at the main venue and only top 6 teams will enter into the next round. In next round all will perform offered physical tasks and the best minimum time will lead to the next round and others teams will be eliminated and in the third round the teams will play for the tough physical tasks and the winner will be declared based on min. Time taken to complete task.Its a mental & physical task gaming event, where in a group of 3 members will face various levels of physical tasks .

The event consists of III Rounds

Venue: Ganesh Temple

Cryptomania:

The event consist of 2 rounds:First round -Elimination round, which consists of multiple choice questions.Second round-Cracking the password and the code using given details.

A team consists of 2 members. Venue:Department of E&C , Block 6